IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	Guanging Yin
Serial No.	10/623,992
Filing Date:	July 21, 2003
Examiner:	2817
Group Art Unit:	Shingleton, Michael B.
Title:	VOLTAGE CONTROLLED OSCILLATOR FOR USE IN PHASE LOCKED LOOP

Mail Stop: Petitions
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Certification Under 37 C.F.R. 1.8

Date of Mailing or Facsimile Transmission: November 8, 2007

I hereby certify that I have caused the document indicated herein to be deposited with the United States Postal Service to Addressee via First Class Mail with sufficient postage for mailing under 37 CFR § 1.8 on the date indicated above and addressed to Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, or transmitted via facsimile to the U.S. Patent and Trademark Office at (571) 273-8300.

Robert A. McLauchlan

PETITION TO WITHDRAW HOLDING OF ABANDONMENT

Dear Sir:

In response to the Notice of Abandonment mailed on April 5, 2007 regarding the above-captioned patent application, the applicant respectfully petitions to withdraw the holding of abandonment because applicant contends that a proper response was made to an Office Action mailed July 31, 2006.

STATEMENT

In the present application, Office Action was mailed July 31, 2007. In response to this Office Action, the undersigned attorney, filed an Amendment by Facsimile Transmission on December 31, 2006 as attached. An Auto Facsimile Transmission Reply was received on December 31, 2006 as acknowledgement of this transmission. The entry of this Amendment was to be made by normal procedures at the Patent Office.

A Notice of Abandonment in this Application was mailed April 5, 2007, for reason of "Applicant's failure to timely file a proper reply to the Office letter mailed on 31 July 2006." The undersigned attorney has reviewed PAIR. Because PAIR indicates that no letter was received in this Application on 31 December 2006, the undersigned attorney presumes that the Application is Abandoned for a PRESUMED failure of Applicants to respond to the Office Action mailed 31 July 2006.

Applicants' attorney (the undersigned) respectfully points out that he did respond to the Office Action mailed July 31, 2006 and that the Office failed to make appropriate entry of the Election in the record.

Because the present Application went abandoned through no fault of the Applicants, the Applicants believe that the statement and showing above are sufficient to support the withdrawal of the abandonment of the present applicant and respectfully petitions that such abandonment be withdrawn.

The Examiner is invited to contact the undersigned by telephone or facsimile if the Examiner believes that such a communication would advance the prosecution of the present invention. No additional fee is due.

The Commissioner is hereby authorized to charge any fees or credit any overpayments to Deposit Account No. 50-2126 of Garlick Harrison & Markison, LLP.

Respectfully submitted,

By:_____

Robert A. McLauchlan, Reg. No. 44,924

Dated: November 8, 2007

Garlick, Harrison & Markison, LLP
P.O. Box 160727
Austin, Texas 78716-0727
(512) 339-4100
(512) 692-2529 (Fax)

USPTO 12/31/2006 12:02:02 PM PAGE 1/001 Fax Server

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Received Cover Page :======>

To: Page 1 of 10 2006-12-31 16:20:41 (GMT) 512-692-2529 From: Robert McLauchlan

BP 2517 10/623,992

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Alexandria, VA 22313-1450

Certification Under 37 C.F.R. 1.8
Date of Mailing or Facsimile Transmission: December 31, 2006
I hereby certify that I have caused the document indicated herein to be deposited with the United States Postal Service to Addressee via First Class Mail with sufficient postage for mailing under 37 CFR § 1.8 on the date indicated above and addressed to Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, or transmitted via facsimile to the U.S. Patent and Trademark Office at (571) 273-8300.

Robert A. McLauchlan

RESPONSE TO OFFICE ACTION

Dear Sir:

Applicant hereby responds to the Office Action mailed July 31, 2006.

PAGE 1/10 * RCVD AT 12/31/2006 11:20:45 AM [Eastern Standard Time] * SVR:USPTO-EFXRF-1/21 * DNIS:2738300 * CSID:512-692-2529 * DURATION (mm-ss):00-44

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Robert A. McLauchlan

RESPONSE TO OFFICE ACTION

Dear Sir:

Applicant hereby responds to the Office Action mailed July 31, 2006.

IN THE CLAIMS:

1. (Original) A high speed bit stream data conversion circuit comprising:

a first data conversion circuit that receives at least one first bit stream at a first bit rate and a corresponding first bit stream data clock and that produces at least one second bit streams at a second bit rate, wherein the number and bit rate of the at least one first bit stream and the at least one second bit stream differ; and

a clock circuit that produces a Reference Clock Signal based on a plurality of inputs that include the first bit stream data clock, wherein the Reference Clock Signal is used to latch the at least one first bit stream, wherein the clock circuit comprises:

a phase locked loop (PLL) having a phase detector that receives the first bit stream data clock and a loop output, a charge pump, a loop filter, a Voltage Controlled Oscillator (VCO), and a divider, wherein the VCO comprises a pair of cross-coupled transistors, an inductor coupled to the cross-coupled transistors, and a filtering circuit having a capacitor and a variable resistor.

2. (Original) The high-speed bit stream data conversion circuit of Claim 1, wherein the filtering circuit reduces noise contained within a bias voltage provided to the VCO.

3. (Original) The high speed bit stream data conversion circuit of Claim 1, wherein the filtering circuit reduces 1/f noise and white noise.

4. (Original) The high speed bit stream data conversion circuit of Claim 1, wherein the resistor within the filtering circuit acts to reduce the voltage applied to the VCO core.

5. (Original) The high-speed bit stream data conversion circuit of Claim 1, wherein the VCO circuit further comprises a second resistor to adjust VCTR voltage.

6. (Original) The high speed bit stream data conversion circuit of Claim 1, wherein the plurality of inputs further comprise:

a Loop Timing Clock Signal;

an External Reference Clock Signal; or

a Reverse Clock Signal provided by an external data conversion circuit.

7. (Withdrawn) The high speed bit stream data conversion circuit of Claim 1, wherein the first data conversion data conversion circuit multiplexes the at least one first bit stream into the at least one second bit stream.

8. (Withdrawn) The high speed bit stream data conversion circuit of Claim 7, further comprising a second data conversion data conversion circuit that receives the at least one second bit stream at the second bit rate and multiplexes into at least one third bit streams at a third bit rate, wherein the number of the at least one third bit streams is less than the number of the at least one second bit streams, and the bit rate of the at least one third bit stream and exceeds the bit rate of the at least one second bit stream.

9. (Withdrawn) The high speed bit stream data conversion circuit of Claim 8, wherein a selectable forward/reverse clock relationship exists between the first data conversion data conversion circuit and the second data conversion circuit.

10. (Original) The high speed bit stream data conversion circuit of Claim 1, wherein the clock circuit further comprises a phase detector operable to generate a phase adjustment signal to the first data conversion circuit.

11. (Original) The high speed bit stream data conversion circuit of Claim 1, wherein the first data conversion circuit demultiplexes the at least one first bit stream into the at least one second bit stream.

12. (Original) The high speed bit stream data conversion circuit of Claim 11, further comprising a second data conversion circuit that receives the at least one second bit

stream at the second bit rate and demultiplexes the at least one second bit stream into a plurality of third bit streams at a third bit rate, wherein the number of the plurality of third bit streams exceed the number of the at least one second bit streams, and the bit rate of the at least one second bit stream and exceeds the bit rate of the plurality of third bit streams.

13. (Original) The high speed bit stream data conversion circuit of Claim 12, wherein a switchable master/slave relationship exists between the first data conversion circuit and the second data conversion circuit.

14. (Original) The high speed bit stream data conversion circuit of Claim 13, wherein the clock circuit further comprises a phase detector operable to generate a phase adjustment signal to the first data conversion circuit.

15. (Canceled):

16. (Canceled):

17. (Canceled)

18. (Canceled)

19. (Canceled)

20. (Canceled)

21. (Original) A method of producing a Reference Clock Signal, within a clock circuit, wherein the Reference Clock Signal is used to latch data between at least one first bit stream and at least one second bit stream, wherein the number and bit rate of the at least one first bit stream and the at least one second bit stream differ, comprising the steps of:

generating with a Voltage Controlled Oscillator (VCO) one of a plurality of inputs to a Phase Locked Loop (PLL) within the clock circuit, wherein the plurality of inputs to the PLL include a first bit stream data clock, and wherein the input provided by the VCO comprises a VCO Output Signal;

reducing noise contained within the VCO Output Signal with a filtering circuit coupled to the VCO, wherein the filtering circuit has a capacitor and a resistor;

selecting from the plurality of inputs to the PLL, an input from which the Reference Clock Signal will be generated; and

generating within the clock circuit, the Reference Clock Signal from the selected input.

22. (Original) The method of Claim 21, further comprising the steps of providing a Loop Timing Clock Signal, an External Reference Clock Signal, and/or a Reverse Clock Signal as the plurality of inputs to the PLL.

23. (Original) The method of Claim 21, wherein the noise contained within the VCO Output Signal is within a bias voltage provided to the VCO.

24. (Original) The method of Claim 21, wherein the step of reducing 1/f noise and white noise from a bias current reduces noise contained within the VCO Output Signal.

25. (Original) The method of Claim 21, further comprising the step of reducing the voltage applied to the VCO core with the resistor of the filtering circuit and a voltage adjusting resistor.

26. (Withdrawn) The method of Claim 24, wherein the Reference Clock Signal is generated within a multistage data conversion circuit used to multiplex at least one first bit streams to at least one second bit stream.

27. (Original) The method of Claim 24, wherein the Reference Clock Signal is generated within a multistage data conversion circuit used to demultiplex at least one first bit streams to at least one second bit stream.

REMARKS

Applicants appreciate the time taken by the Examiner to review Applicants' present application. This application has been carefully reviewed in light of the Official Action mailed July 31, 2006. Applicants respectfully request reconsideration and favorable action in this case.

NONSTATUTORY DOUBLE PATENTING REJECTION

Claims 1-6, 10-14, 21-25 and 27 stand provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-27 of U.S. Patent No. 6,909,332 in view of Gupta 6,362,698. The examiner states:

> The claims of the '332 patent are directed to the same basic multiplexer subcombination and the demultiplexer sub-combination. However, these claims are silent on the use of a vco that has filtering circuit composed of a capacitor and variable resistor. Note that the elected invention of figure 8A only has a FET 406 and this accordingly to applicant has a capacitor and variable resistor structure. Gupta discloses that a vco having a capacitor and variable resistor structure is well known in the art. Note the FETs M7 and M8. This clearly like that of applciant's figure 8A provides for a filtering function thereby enhancing the function of the vco. Thus it would have been obvious to add a vco with a filter function to the claimed invention of the '332 as this is well known for enhancing the function of the vco as taught by Gupta. In other words the addition of a vco that has a filter function does not present a patentable distinction over the claimed vco of the '332 patent. Also note that the claimed method claims that include claim 21 of the instant application is a result of the structure made obvious above and accordingly, these claims cannot form a patentable distinction over the invention made obvious above.

The applicant respectfully traverses the examiner's assertion regarding nonstatutory obviousness-type double patenting. Although the applicant respectfully traverses the nonstatutory double patenting rejection as stated above, the applicant respectfully submits a terminal disclaimer to overcome the provisional rejection based on nonstatutory double patenting.

A two (2) month extension is requested with the appropriate fee is attached. While Applicants believe no other fees are due with this transmission, if any fees are due, the Commissioner is hereby authorized to charge Deposit Account No. 50-2126 of Garlick, Harrison & Markison, LLP.

Please associate this application with customer number 51472.

If the Examiner has any questions or comments, or if further clarification is required, it is requested that the Examiner contact the undersigned at the telephone number listed below. Please reference Attorney Docket No. BP2517.

Respectfully submitted,

Robert A. McLauchlan
Reg. No. 44,924

Date: December 31, 2006

ATTORNEY FOR APPLICANTS

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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

TERMINAL DISCLAIMER TO OBVIATE A DOUBLE PATENTING REJECTION OVER A "PRIOR" PATENT

Docket Number (Optional)
BP 2517

In re Application of: Guanging Yin

Application No.: 10/623,992

Filed: July 21, 2003

For: Broadcom Corporation

The owner*, Broadcom Corporation, of 100 percent interest in the instant application hereby disclaims, except as provided below, the terminal part of the statutory term of any patent granted on the instant application which would extend beyond the expiration date of the full statutory term **prior patent** No. 6,909,332 as the term of said prior patent is defined in 35 U.S.C. 154 and 173, and as the term of said **prior patent** is presently shortened by any terminal disclaimer. The owner hereby agrees that any patent so granted on the instant application shall be enforceable only for and during such period that it and the **prior patent** are commonly owned. This agreement runs with any patent granted on the instant application and is binding upon the grantee, its successors or assigns.

In making the above disclaimer, the owner does not disclaim the terminal part of the term of any patent granted on the instant application that would extend to the expiration date of the full statutory term as defined in 35 U.S.C. 154 and 173 of the **prior patent**, "as the term of said **prior patent** is presently shortened by any terminal disclaimer," in the event that said **prior patent** later:

expires for failure to pay a maintenance fee;
is held unenforceable;
is found invalid by a court of competent jurisdiction;
is statutorily disclaimed in whole or terminally disclaimed under 37 CFR 1.321;
has all claims canceled by a reexamination certificate;
is reissued; or
is in any manner terminated prior to the expiration of its full statutory term as presently shortened by any terminal disclaimer.

Check either box 1 or 2 below, if appropriate.

1. ☐ For submissions on behalf of a business/organization (e.g., corporation, partnership, university, government agency, etc.), the undersigned is empowered to act on behalf of the business/organization.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

2. ☑ The undersigned is an attorney or agent of record. Reg. No. 44,924

/Robert A. McLauchlan, Reg. No. 44,924/ — Signature
12/31/2006 — Date

Robert A. McLauchlan — Typed or printed name

512-339-4100 — Telephone Number

☑ Terminal disclaimer fee under 37 CFR 1.20(d) included.

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*Statement under 37 CFR 3.73(b) is required if terminal disclaimer is signed by the assignee (owner).
Form PTO/SB/96 may be used for making this certification. See MPEP § 324.